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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application

Inventor	:	Farkas
Application No.	:	09/932,086
Filed	:	08/17/2001
For	:	ARRANGEMENT FOR TESTING INTEGRATED CIRCUITS

APPEAL BRIEF

On Appeal from Group Art Unit 2133

Date: 05/27/2007

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Michael Ure
(Name)

M Ure 5/29/07
(Signature and Date)

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NONE

I. REAL PARTY IN INTEREST

The real party in interest is NXP B.V., the successor in interest to the present assignee of record of the present application, Koninklijke Philips Electronics N.V., and not the party named in the above caption.

II. RELATED APPEALS AND INTERFERENCES

With regard to identifying by number and filing date all other appeals or interferences known to Appellant which will directly effect or be directly affected by or have a bearing on the Board's decision in this appeal, Appellant is not aware of any such appeals or interferences.

III. STATUS OF CLAIMS

Claims 2, 4, 5 and 10-14 are pending, all of which stand finally rejected and form the subject matter of the present appeal. Claims 1, 3 and 6-9 have been canceled.

IV. STATUS OF AMENDMENTS

All amendments have been entered. No amendment after final rejection has been submitted.

V. SUMMARY of the CLAIMED SUBJECT MATTER

The present invention relates to the testing of *logic* (as opposed to memory) integrated circuits (ICs). Such testing has in the past typically required either a large test vector memory external to the IC (prior art Fig. 1) or an integrated test vector generator

(prior art Fig. 2). The former approach increases test system complexity and cost. The latter approach increases chip area and hence chip cost.

The present invention takes a different approach to the testing of logic integrated circuits. In this approach, a test vector generator for generating test vectors for the logic integrated circuit is provided external to the IC. The test vectors generated external to the chip are applied to the chip to exercise the functions of the chip. Test results are applied to a response analyzer, that may be located on-chip (Figure 3) or external to the chip (Figure 4). By generating the test vectors (rather than storing them in advance), the need for a large test vector memory is eliminated. Furthermore, by locating the test vector generator external to the IC, chip area is saved and the cost of the IC is reduced.

Claim 10 relates to the tester itself. As recited in independent claim 10, a tester is provided for testing logic circuitry of an integrated circuit, comprising a programmable test vector generator for generating test vectors for the logic circuitry.

The following analysis of independent claim 10 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
10. A tester for testing logic circuitry of an integrated circuit, comprising	Fig. 3, 2; Fig. 4, 2.	Page 4, line 18 to page 5, line 4.
a programmable test vector generator for generating test vectors for the logic circuitry.	Fig. 3, 4; Fig. 4, 4.	Page 4, lines 20-23; page 4, lines 31-34.

Claim 11 relates to an integrated circuit to be tested. As recited in independent claim 11, an integrated circuit comprises means for receiving from an external tester test vectors for testing logic circuitry, and means for receiving from the logic circuitry test

results in response to the test vectors, for producing a compact representation of said test results, and for outputting said compact representation to the external tester.

The following analysis of independent claim 11 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
11. An integrated circuit comprising:	Fig. 3, 1.	Page 4, line 18 to page 4, line 28.
means for receiving from an external tester test vectors for testing logic circuitry; and	Fig. 3, 8.	Page 4, lines 21-23.
means for receiving from the logic circuitry test results in response to the test vectors, for producing a compact representation of said test results, and for outputting said compact representation to the external tester.	Fig. 3, 5.	Page 4, lines 23-28.

Claim 12 relates to a method of testing integrated circuits. As recited in independent claim 12, a method is provided of testing logic circuitry of an integrated circuit, comprising generating within an external tester test vectors for the logic circuitry, using a programmable test vector generator, and the integrated circuit receiving the test vectors and applying the test vectors to the logic circuitry.

The following analysis of independent claim 12 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
12. A method of testing logic circuitry of an integrated circuit, comprising:	Fig. 3, 2; Fig. 4, 2.	Page 4, line 18 to page 5, line 4.
generating within an external tester test vectors	Fig. 3, 4; Fig. 4, 4.	Page 4, lines 20-23; page 4, lines 31-34.

for the logic circuitry, using a programmable test vector generator; and		
the integrated circuit receiving the test vectors and applying the test vectors to the logic circuitry.	Fig. 3, 5; Fig. 4, 5.	Page 4, lines 23-28 and 32-34.

VI. GROUNDS of REJECTION to be REVIEWED ON APPEAL

The issues in the present matter are whether:

1. claims 2, 4 and 10-14 are unpatentable under 35 U.S.C. 103(a) over Abramovici and IBM Tech.

VII. ARGUMENT

I. Rejection of Claims 2, 4 and 10-14 as Unpatentable Over Abramovici in view of IBM Tech.

The first sentence of the rejection mischaracterizes the primary reference, IBM Tech, stating that "IBM Tech substantially discloses an *external tester 60* that generates logic test patterns/vectors to test/diagnose the logic circuitry of plural semiconductor *chips 120* to enable fault localization." This statement is not correct.

Logic test patterns/vectors operate to exercise functions of an integrated circuit for purposes of testing the same. In IBM Tech, when the integrated circuit 20 is "tested," it is in fact *disabled* using a DISABLE GATE input. Other circuitry (40, 50, 60) is *substituted for* the integrated circuit 20. The substituted circuitry does not produce logic test patterns/vectors; rather, it produces the signals that the integrated circuit 20 was intended to produce. If the system functioned incorrectly with the integrated circuit 20 enabled but functions correctly with the integrated circuit 20 disabled and other circuitry substituted therefore, then the integrated circuit 20 may be identified as faulty, and fault localization (to the chip level) will have been achieved. Clearly, however, the integrated circuit 20 is not tested by exercising the functions thereof.

The rejection further states (erroneously) that "[I]t would have been obvious...to modify the procedure in IBM Tech by including therein programmable test pattern circuitry for external application of test data as taught by Abramovici et al, because such modification would provide...a technique whereby 'TPG (test pattern generation) is external to the semiconductor and hence not part of the functional circuitry. ...' to also thereby reduce tester hardware overhead."

As explained above, there is no test pattern generation in IBM Tech. The signal generation performed in IBM Tech may be more appropriately described as *emulation signal generation*. Moreover, such signal generation is clearly *already* performed external to the semiconductor (which is disabled), defeating the foregoing stated motivation to combine the teachings of the references.

With regard to dependent claims 2, 4, 5, 13 and 14, these claims depend from independent claim 1, which has been shown to be patently distinguishable over the cited reference. Accordingly, these claims are also patently distinguishable and allowable over the cited references by virtue of their dependency upon an allowable base claims.

In view of the above, applicant submits that all of the above referred-to claims are patentable over the teachings of the cited references.

VIII. CONCLUSION

In view of the above analysis, it is respectfully submitted that the referenced teachings, whether taken individually or in combination, fail to anticipate or render obvious the subject matter of any of the present claims. Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

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IX. APPENDIX: THE CLAIMS ON APPEAL

2. The integrated circuit of claim 11, wherein the means for receiving test results comprises a test response analysis unit for compressing test response vectors, the integrated circuit further comprising a test control block for controlling the test procedure.

4. The tester of claim 10, comprising a test response analysis unit arranged to compress test response vectors received from the integrated circuit to be tested.

5. The tester of claim 10, wherein the programmable test vector generator is a programmable algorithmic test vector generator which includes an arithmetic and logic unit and generates test vectors in real time.

10. A tester for testing logic circuitry of an integrated circuit, comprising a programmable test vector generator for generating test vectors for the logic circuitry.

11. An integrated circuit comprising:

means for receiving from an external tester test vectors for testing logic circuitry; and

means for receiving from the logic circuitry test results in response to the test vectors, for producing a compact representation of said test results; and for outputting said compact representation to the external tester.

12. A method of testing logic circuitry of an integrated circuit, comprising:

generating within an external tester test vectors for the logic circuitry, using a programmable test vector generator; and

the integrated circuit receiving the test vectors and applying the test vectors to the logic circuitry.

13. The method of claim 12, wherein the integrated circuit includes a test response analysis unit, further comprising:

receiving from the logic circuitry test results in response to the test vectors;

producing a compact representation of said test results; and

outputting said compact representation to the external tester.

14. The method of claim 13, wherein said compact representation includes test vectors applied directly to the external tester to enable fault localization on the logic circuitry.

X. APPENDIX: RELATED PROCEEDINGS

NONE

XI. APPENDIX: EVIDENCE

NONE